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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/601,984	06/23/2003	Robert C. Glenn	P15918	9077

28062 7590 08/10/2004

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EXAMINER	
SHIN, MARC L	

ART UNIT	PAPER NUMBER
2836	

DATE MAILED: 08/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/601,984	GLENN, ROBERT C.	
	Examiner	Art Unit	
	Marc L Shin	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> **The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.**

Claims 9-13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With regard to claim 9, the examiner is unclear about what the applicant means by the limitation "determining that a control voltage of the control circuit is less than a first threshold voltage, the first threshold voltage less than the reset voltage".

With regard to claim 10, the examiner is unclear of the metes and bounds of the limitation "substantially zero".

With regard to claim 11, the examiner is unclear of the metes and bounds of the limitation "substantially infinite".

With regard to claim 12, the examiner is unclear about what the applicant means by the limitation "determining that a control voltage of the control circuit is greater than a first threshold voltage, the first threshold voltage greater than the reset voltage".

With regard to claim 13, the examiner is unclear of the metes and bounds of the limitation "substantially zero".

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4, 7, and 8 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Welland et al (6,574,288 B1), El-Hamamsy et al (5,600,187), and Sandstedt (4,259,746).

Welland et al discloses a circuit comprising:

- a plurality of capacitors coupled in parallel, CD0 – CDn (see Figure 7)
- a plurality of capacitor switches, each one of the capacitor switches, S0 – Sn, coupled in series with a respective one of the plurality of capacitors (see Figure 7)

Welland et al does not disclose one or more biasing circuits to independently set each of the plurality of capacitor switches to one of a reset voltage, a first threshold voltage, and a second threshold voltage. Welland et al also does not disclose a plurality of control switches, connected between the discrete control circuit (812) and the inputs of the capacitor switches.

Regarding claims 1 and 8, El-Hamamsy et al teaches a variable capacitor comprising a series capacitance connected in series with a MOSFET, further comprising bias control circuitry for controlling a bias voltage applied to MOSFET in a predetermined range of voltages (column 8 lines 2-5). It can be seen from Figure 6, that the bias voltage range includes first threshold voltage, a second threshold voltage, and a reset voltage which lies between the first and second threshold voltage. This reads on setting the control voltage to one of a reset voltage, a first threshold voltage, and a second threshold voltage.

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the circuit of Welland et al to include a bias control circuit, as taught by El-Hamamsy et al. The motivation would have been to provide a means for varying the amount of capacitance contributed by each individual capacitor to the total capacitance of the system by applying the different bias levels to the gate of each transistor.

Sandstedt teaches an electrical communication system in which a demultiplexer (78) which takes an input signal and demultiplexes the signal to three memory modules (80_1, 80_2, 80_3)(see Figure 3).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the circuit of Welland et al to include the demultiplexer between the controller (812) and the discretely variable capacitance (402), as taught by Sandstedt. The motivation would have been that it is well known in the art that a single line is less expensive to implement than multiple lines.

Regarding claim 2, El-Hamamsy et al discloses a variable capacitor comprising a series capacitance connected in series with a MOSFET, further comprising bias control circuitry for controlling a bias voltage applied to MOSFET in a predetermined range of voltages (column 8 lines 2-5). It can be seen from Figure 8, that the bias voltage range includes first threshold voltage, a second threshold voltage, and a reset voltage which lies between the first and second threshold voltage. This reads on setting the control voltage to one of a reset voltage, a first threshold voltage, and a second threshold voltage.

Regarding claim 3, Welland et al discloses that the voltage controlled oscillator is coupled to the plurality of capacitors by the capacitor switches and that the frequency of oscillation depends on the capacitance provided to the oscillating circuit by the plurality of capacitors (see Abstract).

Regarding claim 4, Welland et al discloses discrete control circuitry that provides a digital control signal to a discretely variable capacitance circuit (see Abstract).

Regarding claim 7, Welland et al discloses a voltage controlled oscillator coupled to a plurality of capacitors by a plurality of capacitor switches (see Figure 7), where in the output signal is based on either a discretely variable capacitance or a continuously variable capacitance (see column 3, lines 39-50).

Claims 5 and 6 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Welland et al, El-Hamamsy et al, Sandstedt, and Hsu et al (6,754,147). Welland et al, El-Hamamsy et al, and Sandstedt disclose a frequency synthesizer having a voltage controlled oscillator with a variable capacitance that includes a discretely variable capacitance in conjunction with a continuously variable capacitance, as disclosed in claim 1 above. Welland et al, El-Hamamsy et al, and Sandstedt do not disclose a charge pump to sink or source a control current to or from the control circuit, the control circuit generating a control voltage based on the control current. Welland et al, El-Hamamsy et al, and Sandstedt also do not disclose a detector to transmit a difference signal to the charge pump.

Regarding claim 5, Hsu et al teaches a charge pump for producing a control current based on a comparison signal, a loop filter for receiving the control current from the charge pump and producing a corresponding control voltage (column 5, lines 1-8).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the frequency synthesizer of Welland et al, El-Hamamsy et al, and Sandstedt to include a charge pump for producing a control current for the purpose of generating a control voltage, as taught by Hsu et al. The motivation would have been to provide an alternate method of applying a voltage to the gate of the capacitor switches in the event that the biasing circuits malfunction.

Regarding claim 6, Hsu et al teaches detector that produces a comparison signal, that is received by the charge pump, to generate the control current based on the comparison signal (column 4 line 65 – column 5 line 8).

It would have further been obvious to one of ordinary skill in the art at the time of the invention to modify the frequency synthesizer of Welland et al, El-Hamamsy et al, and Sandstedt to include a detector circuit that produces a comparison signal, as taught by Hsu et al. The motivation would have been to provide an alternate means for controlling the voltage of the capacitor switches, in the event that the discrete switches malfunction.

Claim 14 is rejected under 35 U.S.C 103 (a) as being unpatentable over Davis (4,893,087), Welland et al, El-Hamamsy et al, Sandstedt, and Wert (6,552,569 B2).

Davis discloses a transceiver application that can utilize a voltage controlled oscillator in combination with a controlled modulus frequency divisor in the phase locked loop to produce the desired output frequency (column 1, lines 12-29). Davis does not disclose:

(a) a plurality of capacitors coupled in parallel

(b) a plurality of capacitor switches, each of one of the capacitor switches coupled in series with a respective one of the plurality of capacitors

(c) one or more biasing circuits to independently set each of the plurality of capacitor switches to one of a reset voltage, a first threshold voltage, and a second threshold voltage

(d) a plurality of control switches, each of the control switches to couple and decouple a respective one of the plurality of capacitor switches to and from a control voltage

(e) a processor to process the data

(f) a double data rate memory in communication with the processor

Regarding 14 (a) and 14 (b), Welland et al teaches a plurality of capacitors coupled in parallel, CD0 – CDn (see Figure 7). Welland et al further teaches a plurality of capacitor switches, each one of the capacitor switches, S0 – Sn, coupled in series with a respective one of the plurality of capacitors (see Figure 7).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the transceiver of Davis to include a plurality of capacitors coupled in parallel, a plurality of capacitor switches, and a plurality of control switches, as taught by Welland et al. The motivation would have been to provide a means for varying the capacitance of an internal element of a voltage controlled oscillator in order to control the frequency of the VCO.

Regarding 14 (c), El-Hamamsy et al teaches a variable capacitor comprising a series capacitance connected in series with a MOSFET, further comprising bias control circuitry for controlling a bias voltage applied to MOSFET in a predetermined range of voltages (column 8 lines 2-5). It can be seen from Figure 6, that the bias voltage range includes first threshold voltage, a second threshold voltage, and a reset voltage which lies between the first and second threshold voltage. This reads on setting the control voltage to one of a reset voltage, a first threshold voltage, and a second threshold voltage.

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the circuit of Welland et al to include a bias control circuit, as taught by El-Hamamsy et al. The motivation would have been to provide a means for varying the amount of capacitance contributed by each individual capacitor to the total capacitance of the system by applying the different bias levels to the gate of each transistor.

Regarding 14 (d), Sandstedt teaches an electrical communication system in which a demultiplexer (78) which takes an input signal and demultiplexes the signal to three memory modules (80_1, 80_2, 80_3)(see Figure 3).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the circuit of Welland et al to include the demultiplexer between the controller (812) and the discretely variable capacitance (402), as taught by Sandstedt. The motivation would have been that it is well known in the art that a single line is less expensive to implement than multiple lines.

Regarding 14 (e) and 14 (f), Wert teaches a processor to process the data, a line network appliance that uses SSTL to drive double data rate in the random access memory on board (column 1, lines 34-40).

It would have further been obvious to one of ordinary skill in the art at the time of the invention to modify the transceiver of Davis to include a processor to process the data and a double data rate memory in communication with the processor, as taught by Wert. The motivation would have been to provide a means for performing complex computing functions through the use of the processor and double data rate memory.

Claim 15 is rejected under 35 U.S.C 103 (a) as being unpatentable over Davis, Welland et al, El-Hamamsy et al, Sandstedt, Wert, and Elzur (6,621,893 B2).

Davis, Welland et al, El-Hamamsy et al, Sandstedt, and Wert disclose a transceiver to transmit and receive data comprising a voltage-controlled oscillator, as discussed in claim 14 above. Davis, Welland et al, El-Hamamsy et al, Sandstedt, and Wert do not disclose that the system further comprises a framer coupled to the transceiver and to the processor, the framer to decapsulate data received by the transceiver and to encapsulate data to be transmitted by the transceiver.

Elzur teaches an encoder and decoder device that encapsulates and decapsulates data packets (column 3 line 66 – column 4 line 3). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the transceiver of Davis, Welland et al, El-Hamamsy et al, Sandstedt, and Wert to include a encoder decoder device that encapsulates and decapsulates data packets, as taught by Elzur. The motivation would have been to provide a means for protecting the data from hackers in a network.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Marc L Shin whose telephone number is 571-272-2267. The examiner can normally be reached on M - F 8AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on 571-272-2800 ext 36. The fax phone

number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Marc L Shin
Art Unit 2836
Examiner

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